In the Claims:

1. (Original) An aqueous composition useful for polishing semiconductor wafers, comprising a nonionic surfactant that suppresses removal rate of silicon carbide-nitride, the nonionic surfactant having a hydrophilic group and a hydrophobic group, the hydrophobic group having a carbon chain length of greater than three and the nonionic surfactant suppresses silicon carbide-nitride removal rate at least 100 angstroms per minute greater than its decrease in silicon nitride removal rate as measured with a microporous polyurethane polishing pad pressure measured normal to a wafer of 13.8 kPa.

2. (Original) The composition of claim 1 wherein the nonionic surfactant is selected from the group comprising alkanoamide, alkyl polyethylene oxide, alkylphenol polyethylene oxide, polyoxyethylenated alkyl amine oxide, polyoxyethylenated polyoxypropylene glycols, alkyl polyglucoside, alkyl carboxylic acid esters, polyoxyethylenated mercaptans, alkyl diglyceride, polyoxyethylenated alkanolamine, polyalkoxylated amides, tertiary acetylenic glycols and a mixture thereof.

3. (Original) An aqueous composition useful for polishing semiconductor wafers, comprising by weight percent, 0 to 30 abrasive, 0 to 15 inhibitor for a nonferrous metal, 0 to 25 oxidizer, 0 to 10 tantalum removal agent selected from the group comprising formamidine, formamidine salts, formamidine derivatives, guanidine derivatives, guanidine salts and mixtures thereof and 0.001 to 5 nonionic surfactant that suppresses removal rate of silicon carbide-nitride and has a hydrophilic group and a hydrophobic group, the hydrophobic group having a carbon chain length of greater than three and the nonionic surfactant suppresses silicon carbide-nitride removal rate at least 100 angstroms per minute greater than its decrease in silicon nitride removal rate as measured with a microporous polyurethane polishing pad pressure measured normal to a wafer of 13.8 kPa and the nonionic surfactant is selected from the group comprising alkanoamide, alkyl polyethylene oxide, alkylphenol polyethylene oxide, polyoxyethylenated alkyl amine oxide, polyoxyethylenated polyoxypropylene glycols, alkyl polyglucoside, alkyl carboxylic acid esters, polyoxyethylenated mercaptans, alkyl diglyceride, polyoxyethylenated alkanolamine, polyalkoxylated amides, tertiary acetylenic glycols and a mixture thereof.

4. (Original) The composition of claim 3 wherein the nonionic surfactant is selected from the group comprising alkanoamide, alkyl polyethylene oxide, alkylphenol polyethylene oxide and a mixture thereof.

5. (Original) The composition of claim 3 wherein the nonionic surfactant is an alkanoamide and the alkanoamide is an acylation product of alkanolamines from the group comprising monoalkanolamine (MAA), dialkanolamine (DAA), trialkanolamine and a mixture thereof.

6. (Original) The composition of claim 5 wherein the alkanolamine is selected from the group comprising diethanolamine, monoethanolamine, triethanolamine, diisopropanolamine, monoisopropanolamine, ethanoisopropanolamine and a mixture thereof; and the hydrophobic group has a carbon chain length of at least six carbon atoms.

7. (Currently amended) The composition of claim 3 wherein the tantalum removal agent is selected from the group comprising guanidine hydrochloride, guanidine sulfate, amino-guanidine hydrochloride, guanidine acetic acid, guanidine carbonate, guanidine nitrate, formamidine~~formonimide~~, formamidinesulfinic acid and a mixture thereof, and the tantalum removal agent is 0.2 to 6 weight percent.

8. (Withdrawn) A polishing method for removing at least one coating layer from a semiconductor substrate comprising:

contacting the semiconductor substrate with a polishing composition, the semiconductor substrate having a silicon carbide-nitride below the at least one coating layer, the polishing composition containing a nonionic surfactant to suppress removal of the silicon carbide-nitride and the nonionic surfactant having a hydrophilic group and a hydrophobic group, the hydrophobic group having a carbon chain length of greater than three;

polishing the semiconductor substrate with a polishing pad to remove the at least one coating layer at a removal rate greater than a removal rate for the silicon carbide-nitride layer as expressed in angstroms per minute; and

stopping the polishing before removing all of the silicon carbide-nitride layer.

9. (Withdrawn) The method of claim 8 wherein the at least one coating layer includes a silicon nitride layer and the polishing removes the silicon nitride layer.

10. (Withdrawn) The method of claim 9 wherein the at least one coating layer includes a tantalum-containing layer and the polishing composition comprises by weight percent, 0 to 30 abrasive, 0 to 15 inhibitor for a nonferrous metal, 0 to 25 oxidizer, 0 to 10 tantalum removal agent selected from the group comprising formamidine, formamidine salts, formamidine derivatives, guanidine derivatives, guanidine salts and a mixture thereof and 0.001 to 5 nonionic surfactant for suppressing removal rate of silicon carbide-nitride and the nonionic surfactant suppresses silicon carbide-nitride removal rate at least 100 angstroms per minute greater than its decrease in silicon nitride removal rate as measured with a microporous polyurethane polishing pad pressure measured normal to a wafer of 13.8 kPa and the polishing removes the tantalum-containing layer.